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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/811,207 | 03/26/2004 | Cheisan J. Yue | P04,0097 (H0005049,SBE 16 | 1964 |

128 7590 11/17/2005

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| EXAMINER | |
|---|---|
| LEWIS, MONICA | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2822 | |

DATE MAILED: 11/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/811,207 | YUE ET AL. | |
| | Examiner | Art Unit | |
| | Monica Lewis | 2822 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *24 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) *20-39* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/05 & 7/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This office action is in response to the election filed October 24, 2005.

### *Election/Restrictions*

2. Applicant's election without traverse of Embodiment I in the reply filed on 10/24/05 is acknowledged.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 3, 4, 7, 8, 11, 12, 15 and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what is meant by the following: a) "the semiconductor mesa comprises a silicon mesa" (See Claims 3, 7, 11 and 15). The specification discloses that the device mesas may comprise different types of devices (For Example: See Page 9 Lines 5-17). There is nothing disclosed about the semiconductor mesa comprising a silicon mesa. Claims 4, 8, 12 and 16 depend directly or indirectly from a rejected claim and are, therefore, also rejected under 35 U.S.C. 112, second paragraph for the reasons set above.

### *Claim Rejections - 35 USC § 103*

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 5, 6, 9, 10, 13, 14 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Librizzi et al. (U.S. Patent No. 6,429,502) in view of Hirabayashi (U.S. Patent No. 5,889,314).

In regards to claim 1, Librizzi et al. ("Librizzi") discloses the following:

a) a semiconductor substrate (40) (For Example: See Figure 2);

b) a buried insulation layer (42) over the semiconductor substrate (For Example: See Figure 2);

c) a semiconductor mesa (28 or 34) over the buried insulation layer (For Example: See Figure 1 and Figure 2); and

d) a guard ring (36 and 38) substantially surrounding the semiconductor mesa, and wherein the guard ring is arranged to provide RF isolation for the semiconductor mesa (For Example: See Figure 1 and Column 5 Lines 55-57).

In regards to claim 1, Librizzi fails to disclose the following:

a) the guard ring is in contact with the semiconductor substrate.

However, Hirabayashi discloses a semiconductor device that has a guard ring that is in contact with the semiconductor substrate (20) (For Example: See Column 4 Lines 60-67 and Column 5 Lines 1 and 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Librizzi to include a guard ring that is in contact with the semiconductor substrate as disclosed in Hirabayashi because it aids in preventing cross-talk noise (For Example: See Column 2 Lines 45-50).

Additionally, since Librizzi and Hirabayashi are both from the same field of endeavor, the purpose disclosed by Hirabayashi would have been recognized in the pertinent art of Librizzi.

In regards to claims 2, 6, 10 and 14, Librizzi discloses the following:

a) the semiconductor substrate comprises a high resistivity semiconductor substrate (For Example: See Column 5 Lines 19-22).

In regards to claims 5 and 13, Librizzi discloses the following:

a) the semiconductor substrate is doped in an area that is contacted by the guard ring (For Example: See Column 5 Lines 15 and 16).

In regards to claim 9, Librizzi discloses the following:

a) an insulating ring (26) between the guard ring and the semiconductor mesa, wherein the insulating ring surrounds the semiconductor mesa (For Example: See Figure 1).

In regards to claim 17, Librizzi discloses the following:

a) the guard ring comprises a low resistivity guard ring (For Example: See Column 6 Line 6).

In regards to claim 18, Librizzi fails to disclose the following:

a) the guard ring comprises a metal guard ring.

However, Hirabayashi discloses a semiconductor device that has a metal guard ring (For Example: See Column 5 Lines 1-14). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Librizzi to include a metal guard ring as disclosed in Hirabayashi because it aids in providing a low resistance (For Example: See Column 5 Lines 1-14).

Additionally, since Librizzi and Hirabayashi are both from the same field of endeavor, the purpose disclosed by Hirabayashi would have been recognized in the pertinent art of Librizzi.

In regards to claim 19, Librizzi fails to disclose the following:

a) the guard ring comprises a tungsten guard ring.

However, Hirabayashi discloses a semiconductor device that has a tungsten guard ring (For Example: See Column 5 Lines 1-14). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Librizzi to

include a tungsten guard ring as disclosed in Hirabayashi because it aids in providing a low resistance (For Example: See Column 5 Lines 1-14).

Additionally, since Librizzi and Hirabayashi are both from the same field of endeavor, the purpose disclosed by Hirabayashi would have been recognized in the pertinent art of Librizzi.

7. Claims 3, 4, 7, 8, 11, 12, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Librizzi et al. (U.S. Patent No. 6,429,502) in view of Hirabayashi (U.S. Patent No. 5,889,314) and Beyer et al. (U.S. Patent No. 5,264,387).

In regards to claims 3, 7, 11 and 15, Librizzi discloses the following:

a) the semiconductor substrate comprises a silicon substrate, wherein the buried insulating layer comprises a buried silicon oxide layer (For Example: See Column 5 Lines 14-18).

In regards to claims 3, 7, 11 and 15, Librizzi fails to disclose the following:

a) the semiconductor mesa comprises a silicon mesa.

However, Beyer et al. ("Beyer") discloses a semiconductor device that has semiconductor mesa that comprises a silicon mesa (For Example: See Column 3 Lines 15 and 16). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Librizzi to include semiconductor mesa that comprises a silicon mesa as disclosed in Beyer because it aids in providing low leakage (For Example: See Column 2 Lines 20-24).

Additionally, since Librizzi and Beyer are both from the same field of endeavor, the purpose disclosed by Beyer would have been recognized in the pertinent art of Librizzi.

In regards to claims 4, 8, 12 and 16, Librizzi discloses the following:

a) the semiconductor substrate comprises a high resistivity semiconductor substrate (For Example: See Column 5 Lines 19-22).

***Conclusion***

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956

ML

November 8, 2005